REMARKS

The Examiner rejected claims 1-3 under a new ground of rejection, namely under 35 U.S.C. 102(e) as being anticipated by Patana; and allowed claims 4-27 in view of prior amendments and remarks by Applicants. Applicants have amended claim 1, line 10 to correct an overlooked antecedent basis problem – there is no antecedent for "error values" so the word "values" has been deleted with attendant grammatical correction which is also consistent with claim 3 that recites "the multiply-accumulated *error*" (emphasis added).

In rejecting claims 1-3 the Examiner states that with respect to claim 1 Patana discloses an inherent method having a step of dividing an oscillating signal (30) having a first frequency according to a sequence of at least three distinct divide ratios to produce a divided signal having a frequency approximating a reference signal frequency (12); and adapting the first frequency to reduce a phase difference between the divided signal and the reference signal wherein a next value in the sequence of divide ratios is determined by accumulating an error between a present value in the sequence of divide ratios and an average value of the sequence of divide ratios, accumulating the accumulated errors, and selecting the next value in the sequence of divide ratios such that the multiply-accumulated error values are maintained within finite bounds. Applicants respectfully traverse this improper and erroneous conclusion by the Examiner.

In contradistinction to Applicants' claimed invention Patana discloses a digital delta sigma modulator (100) in a fractional-N frequency synthesizer that is a third order modulator having three cascaded first order delta sigma modulators

(102, 104, 106), each having an accumulator (110, 132, 152) and a register (118, 138, 158) with the outputs from the first and second accumulators being input respectively to the second and third accumulators and the carry outputs from all three being input to respective differentiation cascade stages (190, 200, 210). The purpose of Patana is to keep the desired fractional division function controlling a multi-modulus divider (MMD) (34) within the interval -1 to +1, i.e., frequency band 100.25 may be 100 + .25 or 101 - .75. For that purpose the first accumulator monitors a sign bit and uses a logic circuit (180) to monitor the direction of the carry output of the first accumulator (underflow or overflow) for input to the output differentiator (194) which controls the division ratio of the MMD. The inputs to the first accumulator are the N-bit control word and a SIGN bit. Neither input includes any connection to the output sequence of the modulator. Also the accumulators do not remain within finite bounds which is why they have overflow outputs. In fact Patana does not work if the accumulators do not overflow because the modulator output is derived solely from the accumulator overflow outputs (C1 & SIGN, C2 and C3). Finally the differentiator 220 that the Examiner equates as an accumulator cannot operate as such because it lacks feedback from an adder output to its input.

Claim 1 recites that the next value in the value of divide ratios is determined by accumulating an error between a present value in the sequence and an average value for the sequence (see Fig. 3, the first accumulator 350 where -MX is accumulated with N). Patana does not accumulate an error between a present value and an average value because Patana does not couple the output sequence OUTPUT of the modulator to the input of the series of accumulators -- the only inputs are N and SIGN. Claim 1 further recites that the accumulated errors are

themselves accumulated (see Fig. 3, accumulators 340, 330) and that the next value in the sequence of divide ratios is selected so that the multiply-accumulated errors are maintained within finite bounds, i.e., no accumulator overflow. As indicated above Patana does not operate without accumulator overflow, i.e., it is based on accumulator overflow rather than an accumulation of errors. Thus Patana neither teaches nor suggests to one of ordinary skill in the art the modulator as recited by Applicant in claim 1. Further claim 3 specifically recites that the multiply-accumulated error is fed back to the first accumulator. Thus claims 1-3 are deemed to be allowable as being neither anticipated nor rendered obvious to one of ordinary skill in the art by Patana.

In view of the foregoing amendment and remarks entry of this amendment and allowance of claims 1-3 are urged, and such action and the issuance of this case together with already allowed claims 4-27 are requested. Should the Examiner maintain the rejection of claims 1-3, entry of this amendment is requested as placing the case in better form for appeal.

Respectfully submitted,
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